ABSTRACT OF THE DISCLOSURE

In a nonvolatile semiconductor memory device capable of controlling a single memory chip similar to a plurality of memory chips, the memory chip has a plurality of EEPROM circuits, each of which includes a control circuit for carrying out a writing sequential control and which share a data bus. Each of the EEPROM circuits has a chip enable terminal CE and a Ready/Busy terminal R/B, so that data writing processes can be carried out in the respective EEPROM circuits in parallel.